EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER

09055630

PUBLICATION DATE

: 25-02-97

APPLICATION DATE

14-08-95

APPLICATION NUMBER

07207114

APPLICANT: HITACHI VLSI ENG CORP:

INVENTOR :

TAUCHI YOSHIO;

INT.CL.

H03F 1/56 G02F 1/01 H03F 3/08

H03F 3/345 H03F 3/45 H04B 10/28

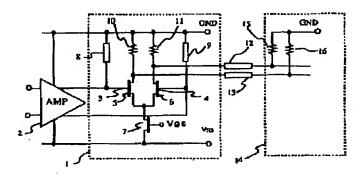
H04B 10/26 H04B 10/14 H04B 10/04

H04B 10/06

TITLE

OUTPUT BUFFER CIRCUIT AND

DRIVER FOR OPTICAL MODULATOR



ABSTRACT :

PROBLEM TO BE SOLVED: To reduce ringing of an output signal without losing an ultrahigh speed performance even when the output buffer circuit is employed in a package of an integrated circuit in which a characteristic impedance of a transmission line such as lead wires does not match a desired impedance with high precision.

SOLUTION: In the buffer circuit 1 that slices an input signal at a prescribed level and providing a resulting output, a filter 8, 9 is provided between a gate terminal 3, 4 of a couple of differential FETs 5, 6 receiving the output signal of an amplifier 2 of a pre-stage and a ground terminal GND. A component of a frequency higher than a frequency of a signal outputted from the output buffer circuit 1 is eliminated among frequency components of signals given to the gate terminals 3, 4 by the filters 8, 9 to suppress ringing of a signal outputted from the output buffer circuit 1 while keeping the high speed performance of an integrated circuit employing the output buffer circuit 1.

COPYRIGHT: (C)1997,JPO